Computer Organization and Architecture – Question 1

Machine Performance and ISA
(a) How do the conditional and unconditional branches impact performance in a pipelined implementation? (15%)

(b) Consider a 4-bit processor and two arbitrary 4-bit positive numbers “a” and “b”. Can we have overflow condition in the following cases? (Just specify Yes or No for each case) (15%)
   i)   a + b;
   ii)  a - b;
   iii) -a - b?

(c) Given the 32-bit pattern (30%)
    0100 1100 1100 0000 0000 0000 0001
What does it represent, assuming that it is
   (i) An unsigned integer number
   (ii) A two's complement integer number
   (iii) An IEEE single precision floating point number (Clue: IEEE Single precision standard floating point numbers have the following format, shown with an example)

\[
\begin{array}{ccccccccc}
0 & 1 & 1 & 1 & 1 & 0 & 1 & 0 & 0 \text{(bit index)}
\end{array}
\]

(d) The speedup resulting from an enhancement is the time to complete a task using the enhancement divided by the time to complete the task without using the enhancement. Use this relationship to answer the following questions. Be sure to write out your calculations clearly.
The base system spends 82% of its time computing and 18% of its time waiting for the disk. During the time that it is computing, the instruction mix and the average cycles per instruction (CPI) for each type is shown in the table below. (40%)

<table>
<thead>
<tr>
<th>Type</th>
<th>Percent of all instructions executed</th>
<th>CPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integer</td>
<td>60%</td>
<td>1</td>
</tr>
<tr>
<td>Floating point</td>
<td>20%</td>
<td>6</td>
</tr>
<tr>
<td>Other</td>
<td>20%</td>
<td>3</td>
</tr>
</tbody>
</table>

On the next page, there are three modifications that can be done to the system. For each modification, compute the speedup resulting from the modification.
(i) The processor is replaced with a new one that reduces the total computation time by 35%.

(ii) The disk is replaced with a solid state device that reduces the disk waiting time by 85%.

(iii) The processor is replaced with a new one that has improved floating point performance. The average floating point CPI is reduced to 3; all other aspects are unchanged.
Computer Organization and Architecture – Question 2

**Memory Hierarchy and Virtual Memory**

a) Suppose a cache contains 1K words (32-bit word) of data. Also suppose the bits of a physical address are interpreted by the cache hardware in the following way:
   - Bits 0-1: byte offset
   - Bits 2-4: word offset
   - Bits 5-12: index
   - Bits 13-31: tag

   What is the degree of associativity in the cache (direct-mapped, 2-way set associative, etc.)? Be sure to explain how you arrived at your answer. (35%)

b) How does a TLB improve memory access performance? (20%)

c) **Virtual memory and TLB:** Consider a virtual memory system with 16 KB pages and 32-bit virtual address space. The physical address space is the same size as the virtual address. A two-way set-associative TLB with a total of 256 entries is used to implement the virtual-to-physical mapping. What is the size of the page table? Show the width of all fields in the TLB and physical address. (45%)