

Altium ***Designer***

**Module 7: Setting Up for Transfer to PCB
and Importing Data**

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Module Seq = 7

7.1 Setting Up for Transfer to PCB

This section outlines how to transfer a schematic design to the PCB Editor using the Synchronizer or a netlist.

7.1.1 Setting the relevant project options

There are a number of settings that control what data is transferred between the schematic design and PCB layout. Select **Project » Project Options** to display the *Options for Project* dialog and click on the **Comparator** tab.

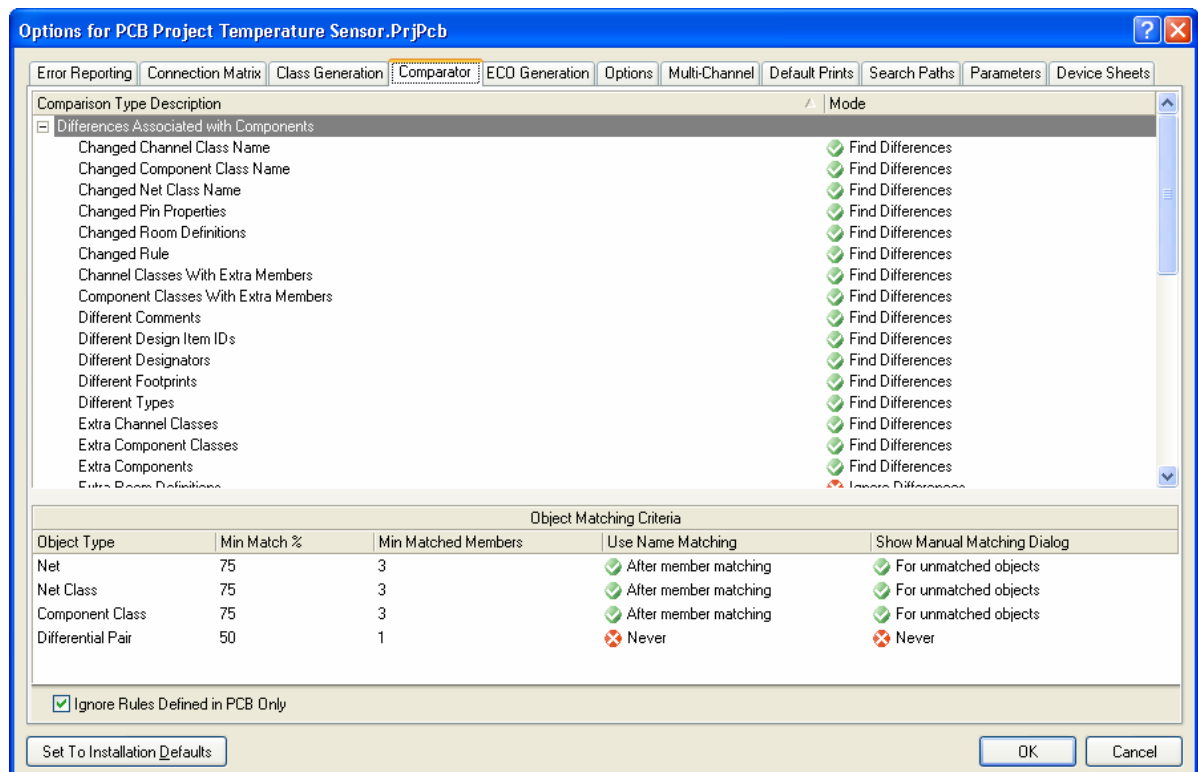


Figure 1. The Comparator options define what information is transferred to PCB.

By default, all options are on. For a simple design such as the training design, you might not want Placement Rooms to be created for each schematic sheet.

7.1.2 Transferring a design to the PCB Editor

- If you are using Altium Designer's PCB Editor to do the board layout, the best method of transferring design information between the schematic and the PCB (and from the PCB back to the schematic) is the Design Synchronizer. Using the Synchronizer, there is no need to create a netlist in the schematic and load that netlist into the PCB. Selecting **Design » Update PCB** will start the synchronization process.
- When you have a PCB and select this command, the *Engineering Change Order* dialog will be displayed. This lists all the changes that must be made to the PCB to get it to match the schematic. This process will be covered in detail during the PCB training module.
- You can also transfer the design using the **Project » Show Differences** command. This uses the design synchronizer, but gives more comprehensive control of the transfer process.

7.1.3 Netlist formats

A netlist is an ASCII file that contains the component and connectivity information defined in the schematic. The netlist can be used to transfer component and connectivity information to other design tools, including PCB Design packages from other vendors. Note that you can still use it to transfer to Altium Designer's PCB editor, but since it does not include unique component ID information it is an inferior method of design transfer.

Netlists are generated by using the **Design » Netlist for Project** menu. By default, there are 25 netlist formats in the menu, including EDIF, Xspice and Multiwire.

7.1.4 Design transfer using a netlist

For most situations, the Synchronizer has superseded netlist loading. In cases where the PCB is being designed from a schematic drawn on another EDA vendor's schematic editor, a netlist can be used.

Using the difference engine, the component and connectivity information in the netlist can be compared to the PCB.

Using a netlist is not as powerful as direct synchronization since during direct synchronization components on both the schematic and PCB is issued with a unique ID (UID). By using UIDs, the designators are not required as the synchronization link and can be changed at will on both sides.

7.1.4.1 Loading a netlist

To load a netlist:

- Select the **Project » Show Differences** menu command. This displays the *Choose Documents to Compare* dialog.
- Enable the **Advanced** check box, as shown in Figure 2.

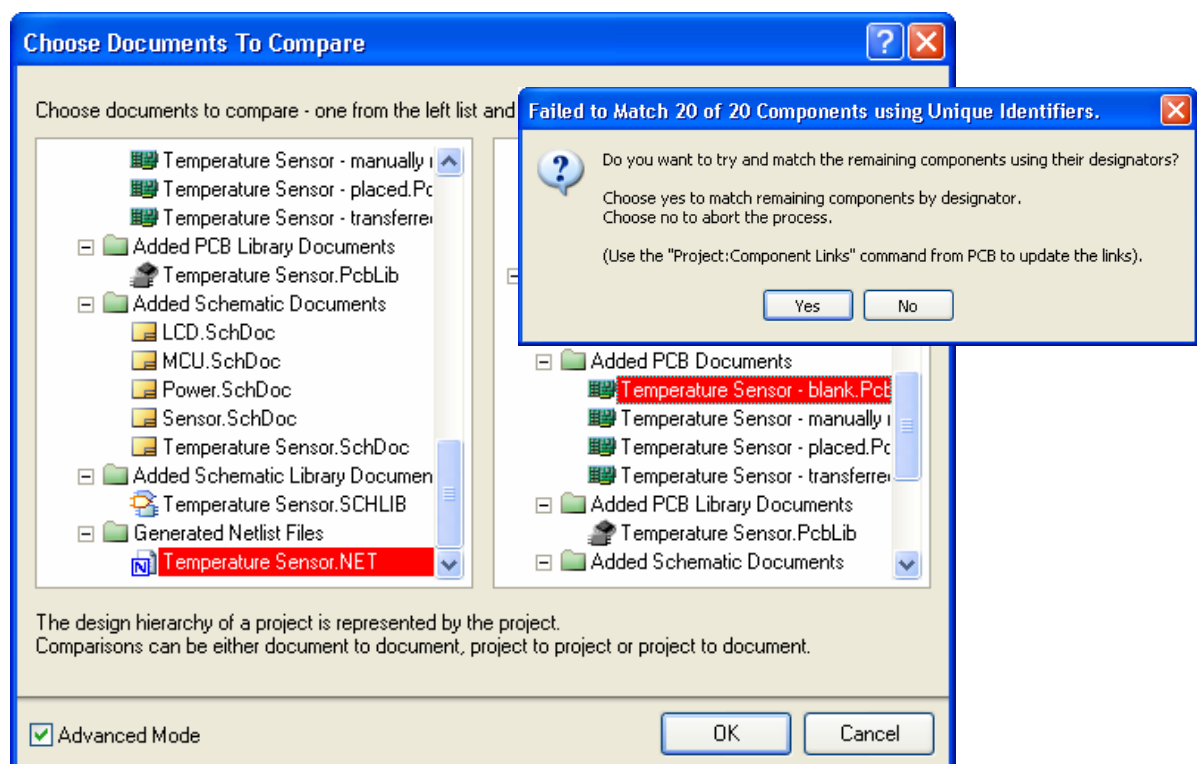


Figure 2. Advanced mode chosen in the Choose Documents to Compare dialog

- Select the required Netlist on one side and the PCB on the other. The Netlist must either be open in Altium Designer or included in the Project.
- When you click **OK**, the *Confirm* dialog will indicate that it is unable to match using UIDs. Click **Yes** to proceed using designators to match by.
- The *Difference* dialog will appear from where the process is the same as direct synchronization.

7.1.5 Exercise – setting project options for design transfer

1. Open the *Options for Project* dialog, and display the **Comparator** tab.
2. Set the Extra Room Definitions option to **Ignore Differences**.
3. Close the dialog and save the project.