PH.D. QUALIFYING EXAM (SPRING 2007)
(Area: Computer Organization and Architecture)

Problem I – Performance, Arithmetic, Pipelining and I/O

A) (15%) Assume a particular function in the latest 3D game contains 1 million instructions, breaking down into the following: 15% stores, 15% loads, 30% branches, 10% integer arithmetic and 30% floating point operations. Given a personal computer running at 3.0 GHz and that load and arithmetic instructions require one cycle, stores require two cycles, branches require four cycles and floating point instructions requires ten cycles, how long will it take for this particular function to finish (in milliseconds, assuming a single-issue processor with no pipeline stalls)?

B) (30%) For the following computations, assume 8-bit signed 2's complement with overflow detection (when this occurs, note it):

a. What is the binary representation of 6 + 13?
b. What is the binary representation of 80 + 70?
c. What is the binary representation of –80 + -70?

C) (40%) Using the standard IF-ID-EX-MEM-WB pipeline, for the following code segment, indicate the number of cycles it would take to completely execute. Assume pipeline A does not implement data forwarding and pipeline B implements data forwarding. All instruction execution takes 1 cycle.

```
LW r5, $100(0)
ADD r4, r5, r7
SUB r5, r1, r6
```

Pipeline A: Without data forwarding

Pipeline B: With data forwarding

D) (15%) Consider the following specifications of a disk. If the average queuing delay is 20 ms, then estimate how much time will it take a to read a file of size 100 MB. Ignore controller delay.

Diameter: 3.5"

Formatted capacity: 73.4 GB

Cylinders: 14,100

Bytes / sector: 512

Sectors / track: 424

Rotation per minute (RPM): 10,033

Seek time: 4.0 ms

Data transfer rate: 80 MB/s

PH.D. QUALIFYING EXAM (SPRING 2007)
(Area: Computer Organization and Architecture)

Problem II – Cache and Virtual Memory

A) (30%) Consider a system with a 2K-byte main memory, 256 byte direct mapped cache and line sizes of 16 bytes. How many lines are there? For the above cache, two 128-byte linear data arrays are going to be placed in the cache from main memory. If the first array starts at location 0 and the second array starts at location 320, how many of the cache lines result in conflicts when both arrays are accessed?

B) (40%) Given a 2 Kbytes two-way set associative cache with 16 byte lines and the following code:

```
 float A[1024], B[1024]
for (int i = 0; i < 1000; i++) {
        A[i] = 40 * B[i];
}
```

Compute the overall miss rate (assume each array element occupies 4 bytes). Assume that all variables except arrays A and B reside in registers, and that arrays A and B are placed consecutively in memory. What kind of cache locality is being exploited?

C) (30%) What is the difference between a write-through and a write-back cache? For a program showing a high degree of temporal locality of reference, which would you expect to have better performance?