PH.D. QUALIFYING EXAM (SPRING 2009)
(Area: Computer Organization and Architecture)

Problem I - Instruction Set Architecture Principle, Evaluation and Optimization

a) (30%) Assume the following instruction mix for a MIPS-like RISC instruction set: 15% stores, 20% loads, 25% branches, and 30% integer arithmetic (not including integer multiply), 5% integer shift, and 5% integer multiply. Given a program with 200 instructions and that load instructions require 2 cycles, branches require 4 cycles, integer ALU and store instructions require 1 cycle and integer multiplies require 10 cycles, compute the overall cycles-per-instruction or CPI.

b) (30%) A commonly used compiler optimization can convert multiplies by a constant integer into a sequence of shift and add instructions with equivalent semantics. Given the same parameters of question a), consider such an optimization that converts multiplies by a constant into a sequence of shifts and adds. For this instruction mix, 50% of the multiplies can be converted into shift-add sequences with an average length of 3 instructions. Assuming a fixed clock frequency, compute the new CPI and overall program speedup.

c) (40%) It has been proposed that a register-memory addressing mode should be added to a load-store architecture. The idea is to replace the two instruction sequence

LOAD R1, 0(Rb)
ADD R2, R2, R1

With the single instruction

ADD R2, 0(Rb)

Assume the new instruction will cause the clock cycle period for the entire machine to increase by 5%. The new instruction affects only the clock cycle period and not the CPI for the machine. Assume that LOAD instructions constitute 26% of the instructions executed. What percentage of loads must be eliminated for the machine with the new instruction to have at least the same performance? (Hint: CPU Time= CPI*Clock_Cycle_Period*Instruction_Count)

Problem II – Fundamental of Cache Design

a) (30%) A computer has a main memory of size 64M words and a cache size of 128K words. **Assume that both main memory and cache are word addressed.** What is the address format used to access (1) a fully associative cache with a block size of 2^m words? (2) a set-associative cache with a block size of 64 words and a set size of 8?

b) (30%) Suppose you have a **word-addressed** memory hierarchy system with the following parameters:

Block size = 16 words
Main memory size = 64 blocks
Cache size = 8 blocks

Suppose your cache is set-associative with 4 sets (i.e., 2 cache blocks per set).

The tag values in the cache are:

TAG	Cache Block Number	Set Number
0000	0	0
0100	1	0
1000	2	1
1001	3	1
1100	4	2
1000	5	2
0110	6	3
1101	7	3

Determine cache hits or misses on accessing the following memory addresses: (1) 0x37A and (2) 0x22C. Justify your answers by showing which cache block will be accessed.

c) (40%) Suppose you have a cached computer system with 1M words in main memory and a cache size of 4K words. Assume that the main memory is divided into blocks with each block containing 16 words. **Assume word addressing.** (1) Assume a set-associative cache with 64 sets of 4 cache blocks per set. What set does the address 0x949DA map into? How many bits are there in each cache tag? What is the cache tag for this address? (2) If the cache is fully associative, what is the cache tag for the address 0x949DA?