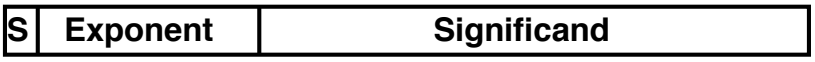
PH.D. QUALIFYING EXAM (SPRING 2012)
(Area: Computer Organization and Architecture)

Question 1. IEEE Standard 754 Floating Point

a) (40%) Single Precision and Double Precision Floating Point, (a) How many total bits for each representation? (b) Please specify the bits for each field (or specify the range of the index of bits). (c) What are the min and max values (exponential format is fine)?

#bits= #bits= #bits=

Single Precision

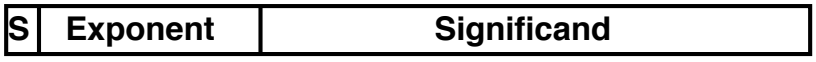


fill up length of each field (above each field)

Total bits=_____
min= _____
max = _____

#bits= #bits= #bits=

Double Precision



fill up length of each field (above each field)

Total bits=_____
min= _____
max = _____

b) (60%) Show the IEEE 754 binary representation of the number -0.75_{ten} in single and double precision (show step-by-step derivations).

Question 2. Memory Hierarchy

a) (40%) Draw the block diagram for address translation and interactions (when hit or miss) among virtual memory, TLB (translation lookaside buffer), cache and physical address. (Hints: memory request from CPU to memory hierarchy)

b) (60%) **b1.** Calculate the CPI of a CPU with a 3-level cache specified as follows. **b2.** Calculate the CPI of the CPU with only 2-level cache. **b3.** Suppose you have only the level 1 cache, calculate the CPI with only 1-level cache. (CPI_1, CPI_2, and CPI_3).

- The ideal CPI of the CPU is 1.1 running at clock rate 500 MHz.
- 1.3 memory accesses per instruction
- Level 1 cache operates at 500 MHz with miss rate of 5% (assuming no cache access cycles for Level 1 cache if hit; if miss, the penalty is the access cycles of the next level cache or memory)
- Level 2 cache operates at 250 MHz with miss rate of 3% and cache access of 2 cycles
- Level 3 cache operates at 100 MHz with miss rate of 1.5% and cache access of 5 cycles
- Memory access penalty is 100 cycles
- (Assuming no additional data transfer overheads.)