PH.D. QUALIFYING EXAM (SPRING 2013)
(Area: Computer Organization and Architecture)

Question 1

(a) A non-pipelined processor takes 9ns to execute an instruction. The latch delay is 0.25ns, and we want our pipelined version of the processor to have 12 stages. What should the clock speed of the processor be? (Assume the work can be evenly divided into 12 stages). (25 %)

(b) Say we have a pipelined machine with 20 stages and a clock speed of 2GHz. The latch delay is 0.15ns. Assume this processor has been perfectly pipelined.

(1) What is the speedup we get on a sequence of 5 instructions executed on this processor (i.e. compared to the un-pipelined version)? Assume there are no dependencies. (25 %)

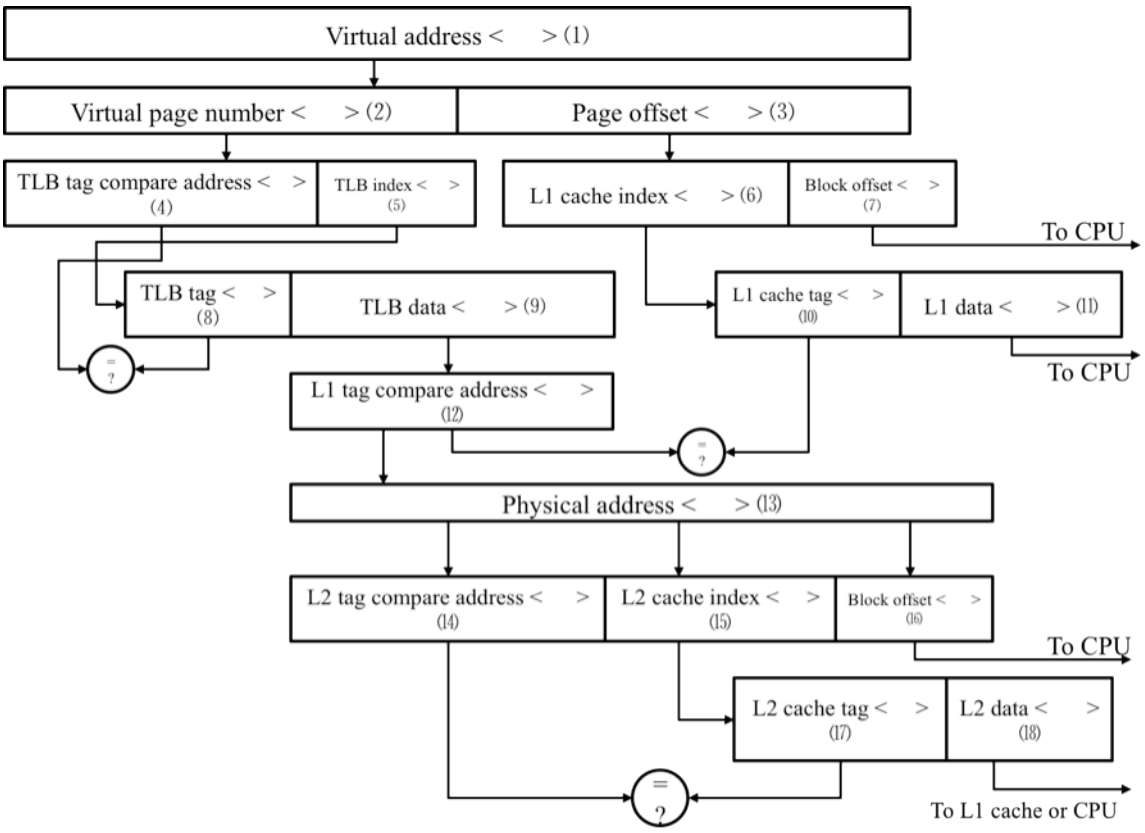
(2) What (ideal) speedup do we get for a much longer sequence of instructions, again assuming no dependencies? (25%)

(3) Assume the same 20-stage pipeline and that it is perfectly pipelined. Clock speed and latch delay can change. At what point does the latch delay cause the speedup to equal 1x? Calculate the latch delay for the speedup of 1x. (25%)

Question 2

(a) A hypothetical computer system has a 32GB byte-addressable virtual memory with a 4MB page size, but only supports 4 GB of physical memory. This system has a 2-level cache architecture with both the L1 and L2 cache using a line size of 32 bytes. The L2 cache is known to be 2-way set associative, with an LRU replacement policy, and 256 KB in size, but the organization of the L1 cache is not given to you. Finally this system employs a direct-mapped TLB consisting of 8 entries.

Below is a schematic presenting the interaction between cache and virtual memory. Fill in the unknown bit-field sizes between the angle brackets < > (**(1) to (18) shown in the Figure below, total 18 places**) (70%)



(b) Consider a 4-way set associative, byte addressable cache. Addresses 0x0000000, 0x0004000, and increasing multiples of 0x0004000 (0x0008000, …) are the only locations that map to set 0. If the line size is 128B, what is the total size of the cache? (30%)