C01A

PH.D. QUALIFYING EXAM (SPRING 2017)
(Area: Computer Organization and Architecture)

Question 1: Machine Performance and ISA

(a) Given the 32-bit pattern **(30%)**

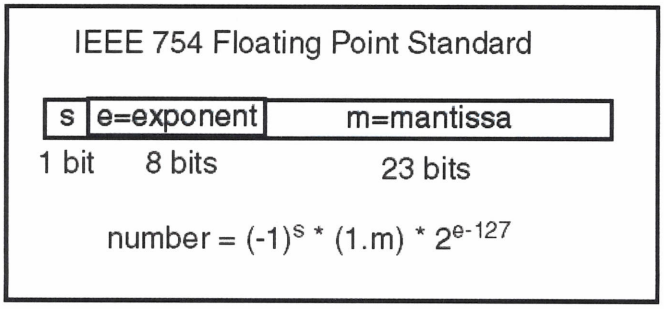
01000000110000000000000000000000

What does it represent, assuming that it is

(i) An unsigned integer number

(ii) A two's complement integer number

(iii) An IEEE single precision floating point number (Clue: IEEE Single precision standard floating point numbers have the following format, shown with an example)



(b) Add the 8-bit unsigned binary numbers A = 11111000 and B = 01101100.

What is the decimal value of the result produced, assuming the result is 8 bits. Has overflow occurred? What is a good way to detect overflow in an adder implementation? **(30%)**

C01B

(c) The speedup resulting from an enhancement is the time to complete a task using the enhancement divided by the time to complete the task without using the enhancement. Use this relationship to answer the following questions. Be sure to write out your calculations clearly. The base system spends 82% of its time computing and 18% of its time waiting for the disk. During the time that it is computing, the instruction mix and the average cycles per instruction (CPI) for each type is below. **(40%)**

Type	**Percent of all instructions executed**	**CPI**
Integer	40%	1
Floating point	30%	5
Other	30%	2

There are three modifications that can be done to the system. For each modification, compute the speedup resulting from the modification.

(i) The processor is replaced with a new one that reduces the total computation time by 35%.

(ii) The disk is replaced with a solid state device that reduces the disk waiting time by 85%.

(iii) The processor is replaced with a new one that has improved floating point performance. The average floating point CPI is reduced to 3; all other aspects are unchanged.

C02

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Question 2: Memory Hierarchy and Virtual Memory

a) A computer system has a 32KB, 8-way set associative cache, and the block size is 8 bytes. The machine is byte addressable, and physical addresses generated by the CPU are 22 bits. Specify how the physical address is partitioned into tag, set, and offset fields, giving the number of bits in each field. **(35%)**

b) What does the processor do on a TLB miss? **(20%)**

c) **Virtual memory and TLB**: Consider a virtual memory system with 16 KB pages and 32-bit virtual address space. The physical address space is the same size as the virtual address. A two-way set-associative TLB with a total of 256 entries is used to implement the virtual-to-physical mapping. What is the size of the page table? Show the width of all fields in the TLB and physical address. **(45%)**