Questions for Digital Logic (January 2007)

Question 1: Consider the function $f = \bar{a}_1 \bar{a}_2 + \bar{a}_2 \bar{a}_3 + a_1 a_2 a_3$.

a. Build a circuit that implements the function using only two 2-input Look-Up-Tables (LUTs). In your answer, show clearly what truth table is implemented inside each LUT.

b. Derive the minimal sum-of-products expression for the function and provide its cost in terms of total number of gates and total number of gate inputs of the corresponding circuit. Assume that each variable and its complement are available as inputs (i.e., you do not need inverters to get $\bar{a}_1$, $\bar{a}_2$ and $\bar{a}_3$ from a_1, a_2 and a_3).

c. Derive the minimal product-of-sums expression for the function and provide its cost in terms of total number of gates and total number of gate inputs of the corresponding circuit.

d. Use Shannon's expansion to derive a multilevel circuit that implements the function and has a lower cost than the cost computed to answer part b. of this question. You are allowed to use only gates of type AND, OR, NAND, NOR and XOR. State what the cost of the multilevel circuit is.

Question 2:

a. Design a counter that counts pulses on a line w and displays the count in the sequence *0, 2, 1, 3, 0, 2 …* using D flip-flops in your circuit. Use w as the clock and call your most significant output z_1 and the least significant output z_0. Similarly, use y_1 and y_0 to represent the current state and Y_1 and Y_0 to represent the next state. You must show the following derivation steps: (1) a 3-column state table, which relates present states to next states to output values, (2) a 3-column state-assigned table, which is the same as the state table with state names replaced by the values of y_1y_0 and Y_1Y_0, (3) the next-state expressions relating Y_1 and Y_0 to y_1 and y_0, and (4) the logic circuit of the counter.

b. Repeat part a. of this question using JK flip-flops instead of D flip-flops. You only need to show (1) the excitation table for JK flip-flops, as derived from the state-assigned table of part a. and (2) the logic circuit. The excitation table is a 4-column table showing the output z_1z_0 of the circuit for different values of the present state y_1y_0 and the possible values of the flip-flop inputs.

c. Repeat part a. of this question using T flip-flops instead of D flip-flops. You only need to show (1) the excitation table for T flip-flops, as derived from the state-assigned table of part a., and (2) the logic circuit. The excitation table is a 4-column table showing the output z_1z_0 of the circuit for different values of the present state y_1y_0 and the possible values of the flip-flop inputs.