DIGITAL LOGIC

[100%] 1. Find the Minimum Sum of Products (MSOP) and Minimum Product of Sums (MPOS) equivalent of the below Boolean expression using K-Maps. Please note /A = ~A = (A Not) i.e., A

[50%]

a.) Z = /A*/B*/D + /A*B*D + A*/B*C*/D + A*B*C*D + /B*/C*/D + B*/C*D

\[ Z_{MSOP} = \ ]

\[ Z_{MPOS} = \ ]

[50%]

b.)

\[ W = (\overline{A} + B + C) * (\overline{A} * \overline{B} * \overline{C}) \]

\[ W_{MSOP} = \ ]

\[ W_{MPOS} = \ ]

\[ \begin{array}{c|c|c|c|c|c|c|c} \hline & BC & & & & & & \\ \hline A & & & & & & & \\ \hline \hline \end{array} \]

\[ W_{MSOP} \]

\[ \begin{array}{c|c|c|c|c|c|c|c} \hline & BC & & & & & & \\ \hline A & & & & & & & \\ \hline \hline \end{array} \]

\[ W_{MPOS} \]
2. Design a system that counts the following sequence: 0, 1, 2, 3, 7, 0 etc. The system must asynchronously reset to count “0” when Start (active-high) goes true. When the count is 3, the active-low output Z should be true. Use a JK-FF for the most significant bit of the counter, a T-FF for the least significant bit, and a D-FF for any other bits you might need. Note: All the given FFs have asynchronous clear and set inputs.

[20%] a) Complete the next-state truth table. Add or remove columns if necessary.

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[50%] b) Find the required simplified equations.

c) On a blank page design the complete counter circuit, minimizing the total number of components, but using the FFs as described in part (a) above. All inputs and outputs of the circuit should be clearly indicated coming into or out of the below box. Your design must include the circuitry necessary to re-start the counter at count “0” asynchronously, when the Start(H) signal goes true.