EEE5322-4310 - VLSI Circuits and Technology 1

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Lectures will be posted here:

Lecture 1

Course Number & Name: EEL 4310 and EEL5322 - Digital Integrated Circuits Design

Credits and Contact Hours: 3 crs; 3 classes per week of 50 minutes each

Instructor's or Course Coordinator's Name: Dr. Scott E. Thompson

Live lecture MWF 7th period 1:55 - 2:45

Course can be completed online but attendance and participation in live lectures is encourage

Classes will generally be recorded live and posted within 1 hour. There will also be a few flipped classes.

zoom link for all classes will be https://ufl.zoom.us/j/7773002921Links to an external site.

Recorded lectures will be posted under "Zoom Conferences" and on home page

Contact info Prof. Scott Thompson

535 Engineering Bldg

846-0320

Office hours: M W F 8th period days of live class

Plus e-learning discussion board (https://lss.at.ufl.edu/)

(plus additional office hours arranged via email thompson@ece.ufl.edu)

Cadence TA

Textbook Title, Author, and Year:

Title - Introduction to Microelectronic Fabrication **(Required)**
Author - Richard C. Jaeger
Publication date and edition - 2nd Edition, Modular Series on Solid State Devices, Volume 5, Prentice Hall
dISBN Number - 0-201-44494-7

Title - Digital Integrated Circuits, A Design Perspective **(Required)**
Author - Jan. M. Rabaey, A. Chandrakasan, and B.Nikolic
Publication date and edition - 2nd Edition, Prentice Hall
ISBN Number - 0-13-090996-3, 2003

Computer and Software required: Workstations with CADENCE Design system on campus, off-campus can use XWindows or X-terminal on a high-speed internet link to UF Campus Computers, or can use equivalent IC design software

1. **Supplemental Material:**

Specific Course Information

1. **Catalog Description:** Fabrication, Layout, Analysis and design of digital and circuits using MOS Transistors
2. **Prerequisites or Co-requisites:** EEL 3396, EEL 3308
3. **Required, Elective, or Selected Elective (Table 5-1):**

Specific Goals for the Course

1. **Specific Outcomes of Instruction:**

This course focuses on analysis and design of modern digital circuits. Silicon technology and transistors are introduced and described from a digital point of view, and the performance of various circuits is derived and estimated. CMOS digital circuits will be designed and analyzed. Students will have a semester long team SRAM chip design project using commercial software Cadance. Project will cover advanced topics such as manufacturing variations.

1. **Explicitly indicate which of the student outcomes listed in Criterion 3 or any other outcomes are addressed by this course:**

EE2, a, c, e, I, k

Topics to Be Coverer

Week 1: Moore's Law, History and Future of Computing, Chipworks tear down of a mobile computer (iPhone and iPad), Jaeger Chapter 1.

Week 2: Design rules, Chap. 2 .1, 2.2 and 2.3 of Rabaey, 1.2, 1.3.1

Week 3: Contacts and Interconnects Chap. 7 Jaeger and handouts. MOS Process Integration Chap. 9 of Jaeger and State of the art CMOS planar and FinFET SOC

process flow: 28nm, 20nm, 14nm, 10nm Logic Technologies and advanced layout issues: Optical Proximity correction and Restrictive Design Rules

Week 4-5: What is VLSI, **Cadence Design Training**, Statistics Review, and Introduction to micro fabrication with emphasis on process variation Chap. 5 .1, 5.2, 5.3, 5.4 of Jaeger, plus handouts and Chipworks reverse engineering reports

Week 6-7: CMOS Logic, DRAM, NAND, CMOS image sensor chips fabrication, bit cell or pixel cell, and array architecture Chap. 8.7 of Jaeger and Chapter 2.2 Rabaey plus handouts

Week 8-9: Layout Layers and X-sections Design Rules, Resistance, Capacitance, MOSFET

Chap. 4.1 to 4.3 and Chap. 3.3 of Rabaey and 9.2, 9.3 Jaeger

Week 10: MOS Transistors, CMOS Inverters, Chap. 3.3 and Chap. 5 of Rabaey

Week 11: CMOS Inverters, Chap. 5 of Rabaey

Week 12: Combination Logic, Compound Gates, Chap. 6 of Rabaey

Week 13: Transmission Gates, Memory, Chap. 6 and Chap. 12 of Rabaey

Week 14: Memory, Pseudo NMOS, Pass Trans. Logic, Chap. 6 of Rabaey

Week 15: Pre-charge Logic, and Dynamic Logic, Chap. 6 of Rabaey

Week 16: Domino Logic, Logic Comparison, Noise Chap. 6 of Rabaey

- Grading:

    Class exams

        100 Points Test 1 Friday Sept. 29

        100 Points Test 2 Friday Oct. 20

        100 Points Test 3 Firday Nov. 17

        200 Points Comprehensive Final: 12/14/2024 @ 10:00 am - 12:00 PM

    Cadences assignment 1 (25 points)

    Group SRAM Design project (100 points) Final Class Project Due last day of class

    Homework 5 points per assignment

- Test and projects and homework different for EEL 4310 and EEL5322
- No exam make-up unless valid excuse. All valid excuses must be approved by the Professor
- Final Grading Scale

- A 100% to 94%, A- < 94% to 90%, B+< 90%to 87%, B< 87% to 84%
- B-< 84% to 80%, C+< 80% to 77%, C< 77% to 74%, C-< 74% to 70%
- D+< 70% to 67%, D< 67% to 64%, D-< 64% to 61%, E< 61% to 0%
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- Attendance: All lecture classes will be record via zoom during the regularly scheduled live class and will be made available online shortly after the lecture. A zoom link will be provided before the lecture. Students are free to attend the live lecture in person, participate in the live lecture over zoom, or watch the posted lecture.

Course Summary:

Date	Details	
Wed Aug 23, 2023	Calendar Event Lecture 1 time of class	1
Fri Aug 25, 2023	Calendar Event Lecture 2 time of class	1
Mon Aug 28, 2023	Calendar Event Lecture 3 RECORDED. — Optional office hours to address all questions	1
Wed Aug 30, 2023	Calendar Event Lecture 4 RECORDED Lecture. NO OFFICE HOURS	1
Fri Sep 1, 2023	Calendar Event Lecture 5 RECORDED lecture. Optional office hours to address all questions	1
Wed Sep 13, 2023	Quiz Cadence Tutorial 1 Assignment	
Fri Sep 15, 2023	Quiz Cadence Tutorial 2 Assignment	
	Assignment Homework 1	
Fri Sep 22, 2023	Quiz Cadence Tutorial 3 Assignment	
Fri Oct 6, 2023	Quiz Cadence Tutorial 4 (Fin 7nm) Assignment	