# Course Syllabus

**EE5320 Analog IC Design I (available on EDGE/ONLINE)**

This course explores the fundamentals of the analog IC design, ranging from single stage amplifiers to switched-capacitor networks and multi-stage frequency compensation schemes. Throughout the semester, the students will be introduced to various critical circuits which the analog IC depends upon. The state of the art applications will be discussed for each of these circuits, and the past and future challenges and the roadmap of analog IC will be tackled. In this course, the students will be introduced to Cadence® platform, an industry preferred simulation and layout engine, not only to analyze the provided circuits, but also to design several commonly used structures including switched-capacitor fully differential opamps. An extensive tutorial to Cadence will be provided to help familiarize the students with this simulation platform.
The course objective is to provide a thorough background of analog circuits, discuss the real world applications, IC design challenges and prepares students for other areas of analog and digital IC design. ***If you plan to pursue career in IC design, either analog or digital, this course is "a must", and it is recommended by ALL IC design companies.***

***Pre-Reqs***

*Electronics Circuits 1 & 2 (or equivalent knowledge of the topic)*

***Recommended***

*Circuits 2*

****If you have not taken these courses and still would like to enroll, please contact me.***

**What you need to know before taking this course:**

- **Basic knowledge of circuits, KVL/KCL, first order systems (RC time constant)**
- **Basic knowledge of large signal and small signal analysis**
- **Basics of MOS transistors (DC/ac) (a detailed review will be provided)**
- **Bode blot and frequency response (short review will be offered)**
- **Fourier and Laplace Transforms**

**Those who want to have a head start:**

Read the first 2-3 chapters of Razavi's Analog CMOS IC textbook (link provided below)

Class location & dates:

**Location: TBD**

**Time: TBD**

**Exams and office hours:**

**Midterm 1: TBD**

**Midterm 2: TBA**

**Final Exam: TBA**

**Office hours:**

**Dr. Maghari: maghari@ece.ufl.edu (mailto:maghari@ece.ufl.edu) Office Hours: TBD**

**TAs:**

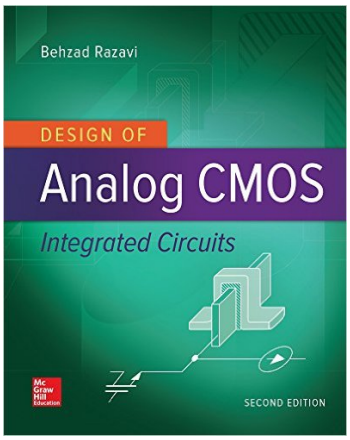
**Yingjie Chen (chenyingjie@ufl.edu) Office Hours: TBD**

**Arun Javvaji (arun.javvaji@ufl.edu) (mailto:pavanterdal@ufl.edu)) Office Hours: TBD**

**Office Hour Location TBD**

***Please put EE5320 in the subject of your email for any email correspondence.***

**Textbooks**




Design of Analog CMOS Integrated Circuits **(2nd edition)**

**(Highly recommended)**

By B. Razavi

Publisher: McGraw-Hill Education; 2 edition (January 20, 2016)
ISBN-10: 0072524936
ISBN-13: 978-0072524932

**Link to Amazon (https://www.amazon.com/Integrated-Circuits-Electronics-Computer-Enginering/dp/0072524936/ref=sr_1_1?ie=UTF8&qid=1498867196&sr=8-1&keywords=Design+of+Analog+CMOS+Integrated+Circuits)**

**Grading basis**

| | |
|---|---|
| **Homework & Cadence** | **25%** |
| **Quiz** | **10%** |
| **Midterm 1** | **20%** |
| **Midterm 2** | **20%** |
| **Extra Credit Quiz** | **5%** |
| **Final Exam (4306)/ Final Project (5320)** | **25%** |
| **Total** | **100%+ 5% extra credit quiz** |

### Course Outline

- Review
  - MOS & *Bipolar* Basics (*Bipolar* is optional and may be discussed at the end of the semester)
    - Large signal
    - Small signal
  - Amplifiers
    - Single Stage
      - Transistor level simulation in Cadence
      - Analog Layout
    - Multi-Stage
  - Cascode and Current mirrors
    - Current mirrors
      - Layout and matching
    - Cascode mirrors and amplifiers
  - Differential circuits
    - Fully Differential OTAs
      - Inter-digit and common-centroid layout
    - Common-mode setting
    - Multi-stage
  - Frequency Response
    - Single-stage
    - Multi-stage OTA
    - Miller compensation
  - Feedback
    - Loop Analysis

    - Frequency Response
    - Non-linearity
  - Voltage and Current References
    - Fixed-Gm Bias
    - Bandgap Voltage Reference
  - Introduction to Switched Capacitor circuits

**About the instructor:**

Nima Maghari received the B.S. degree in electrical engineering from the University of Tehran, Iran, in 2004 and the Ph.D. degree in electrical engineering from Oregon State University in 2010.

He is currently an associate professor at the department of electrical and computer engineering, University of Florida, Gainesville. From 2004 to 2006, he was with IC-LAB, University of Tehran, where he was involved with audio delta-sigma converters and low-voltage bandgap references. In 2008 he was recipient of CICC-AMD outstanding student paper award. He is currently serving as an Associated Editor of IEEE Transactions on Circuits and Systems-I. He has published more than 50 conference and journals papers in IEEE and IEE.

His research interests include high performance analog-to-digital converters, delta-sigma modulators, phased-locked loops, synthesizable analog circuits, time-assisted data conversion techniques and low-power low-voltage regulators.

# Course Summary:

| Date | Details | |
|---|---|---|
| Thu Sep 7, 2017 | **HW1 Due Date : Thursday Sep 7th** (https://ufl.instructure.com/courses/353983/assignments/3586493) | due by 11:59pm |
| Tue Sep 26, 2017 | **Cadence Assignment** (https://ufl.instructure.com/courses/353983/assignments/3586489) | due by 11:59pm |
| Mon Oct 2, 2017 | **HW2** (https://ufl.instructure.com/courses/353983/assignments/3586494) | due by 12pm |
| Thu Oct 12, 2017 | **HW3** (https://ufl.instructure.com/courses/353983/assignments/3586495) | due by 1:55pm |
| Tue Oct 17, 2017 | **Cadence Assignment 2** (https://ufl.instructure.com/courses/353983/assignments/3586490) | due by 5pm |
| Fri Nov 3, 2017 | **HW4** (https://ufl.instructure.com/courses/353983/assignments/3586496) | due by 5pm |

| Date | Details | |
|---|---|---|
| Thu Nov 16, 2017 | **Cadence Assignment 3** (https://ufl.instructure.com/courses/353983/assignments/3586491) | due by 11:59pm |
| Mon Dec 11, 2017 | **Final Project** (https://ufl.instructure.com/courses/353983/assignments/3586492) | due by 9am |