Course Syllabus

Course Number & Name: EEL 4310 and EEL5322 - Digital Integrated Circuits Design

Credits and Contact Hours: 3 credits; 3 classes per week of 50 minutes each

Instructor's or Course Coordinator's Name: Dr. Scott E. Thompson

Contact info

535 Engineering Bldg
846-0320
Office hours: M W F 7th period days of live class

Plus e-learning discussion board (https://lss.at.ufl.edu/)

(plus additional office hours arranged via email thompson@ece.ufl.edu)

TA Yingjie Chen (chenyingjie@ufl.edu)

TA Xiaodong Xu (xu1992@ufl.edu)

TA Office hours: (email to arrange)

Textbook Title, Author, and Year:
Title - Introduction to Microelectronic Fabrication *(Required)*
Author - Richard C. Jaeger
dISBN Number - 0-201-44494-7

Title - Digital Integrated Circuits, A Design Perspective *(Required)*
Author - Jan. M. Rabaey, A. Chandrakasan, and B.Nikolic

Computer and Software required: Workstations with CADENCE Design system on campus, off-campus can use XWindows or X-terminal on a high-speed internet link to UF Campus Computers, or can use equivalent IC design software

1. **Supplemental Material:**

**Specific Course Information**

1. **Catalog Description:** Fabrication, Layout, Analysis and design of digital and circuits using MOS Transistors
2. **Prerequisites or Co-requisites:** Electronics 1 (3308) and Digital Logic (3701C)
3. **Required, Elective, or Selected Elective (Table 5-1):**

**Specific Goals for the Course**

1. **Specific Outcomes of Instruction:**

This course focuses on analysis and design of modern digital circuits. Silicon technology and transistors are introduced and described from a digital point of view, and the performance of various circuits is derived and estimated. CMOS digital circuits will be designed and
analyzed. Students will have a semester long team SRAM chip design project using commercial software Cadance. Project will cover advanced topics such as manufacturing variations.

1. **Explicitly indicate which of the student outcomes listed in Criterion 3 or any other outcomes are addressed by this course:**

   EE2, a, c, e, I, k

**Topics to Be Coverer**

Week 1: Moore’s Law, History and Future of Computing, Chipworks tear down of a mobile computer (iPhone and iPad), Jaeger Chapter 1.

Week 2: Design rules, Chap. 2.1, 2.2 and 2.3 of Rabaey, 1.2, 1.3.1

Week 3: Contacts and Interconnects Chap. 7 Jaeger and handouts. MOS Process Integration Chap. 9 of Jaeger and State of the art CMOS planar and FinFET SOC process flow: 28nm, 20nm, 14nm, 10nm Logic Technologies and advanced layout issues: Optical Proximity correction and Restrictive Design Rules

Week 4-5: What is VLSI, **Cadence Design Training**, Statistics Review, and Introduction to micro fabrication with emphasis on process variation Chap. 5.1, 5.2, 5.3, 5.4 of Jaeger, plus handouts and Chipworks reverse engineering reports

Week 6-7: CMOS Logic, DRAM, NAND, CMOS image sensor chips fabrication, bit cell or pixel cell, and array architecture Chap. 8.7 of Jaeger and Chapter 2.2 Rabaey plus handouts

Week 8-9: Layout Layers and X-sections Design Rules, Resistance, Capacitance, MOSFET
Chap. 4.1 to 4.3 and Chap. 3.3 of Rabaey and 9.2, 9.3 Jaeger

Week 10: MOS Transistors, CMOS Inverters, Chap. 3.3 and Chap. 5 of Rabaey

Week 11: CMOS Inverters, Chap. 5 of Rabaey

Week 12: Combination Logic, Compound Gates, Chap. 6 of Rabaey

Week 13: Transmission Gates, Memory, Chap. 6 and Chap. 12 of Rabaey

Week 14: Memory, Pseudo NMOS, Pass Trans. Logic, Chap. 6 of Rabaey

Week 14: Pre-charge Logic, and Dynamic Logic, Chap. 6 of Rabaey

Week 15: Domino Logic, Logic Comparison, Noise Chap. 6 of Rabaey

- Grading:
  
  Class exams

  100 Points  Test 1  Friday Sept. 20

  100 Points  Test 2  Wednesday Oct. 23

  150 Points  Test 3 Monday Nov. 18

  250 Points  Comprehensive Final as scheduled by college (12:30-2:30 Thursday Dec. 11)
Course Summary:

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- Cadences assignment 1 (25 points)
- Group SRAM Design project (150 points) Final Class Project Due Dec 4 (midnight)
- Homework 10 points per assignment

- Test and projects and homework different for EEL 4310 and EEL5322

- No exam make-up unless valid excuse. All valid excuses must be approved by the Professor.

- Final Grading Scale

- ≥90% → A; ≥86.67% → A-; ≥83.33% → B+; ≥80% → B; ≥76.67% → B-; ≥73.33% → C+; ≥70% → C; ≥66.67% → C-; ≥63.33% → D+; ≥60% → D; ≥56.67% → D-; <56.67% → E

- Attendance: Due to quantity and research nature of material, it is important to make every attempt to attend class or watch all class lectures (when possible).