EEL 4713C – Computer Architecture
Syllabus – Spring 2020

Schedule: Tuesday 7th period 1:55 – 2:45 pm, MCCB 1108
Thursday 7th and 8th period 1:55 – 3:50 pm, MCCB 1108
Thursday 9th through 10th periods 4:05 – 6:00pm, MCCB 2102

Instructor: Ann Ramirez (Gordon-Ross) (anngordonross@ece.ufl.edu)
Benton 319 - Office Hours: By appointment

TAs: **Lecture and homework primary:** James Nall (nallj@ufl.edu)
Office hours – TBA

Lab and assignments primary: Mohammad Farmani (mfarmani@ufl.edu)
Office hours – TBA

Text: "Computer Organization & Design", Patterson & Hennessy, Morgan-Kaufmann, 5th edition, ISBN 0124077269 (The white one with the orange spine)

Topics Covered: Fundamentals in design and quantitative analysis of modern computer architectures and systems, including instruction set architecture, basic and advanced pipelining, superscalar and VLIW instruction-level parallelism, memory hierarchy, storage, and interconnects.

Prerequisites: EEL3701C and EEL 4712: Combinational and sequential logic design principles, advanced modular design logic, finite state machines, and binary logic. Competence in programming with a hardware description language (VHDL or Verilog) is required.

Lab Assignments: Assignments consisting of questions covering the material discussed in class and design laboratories will be posted on the web and announced in class. There will be approximately 6 assignments. These laboratories consist of coding a MIPS assembler/disassembler and designs implemented in VHDL, increasing in complexity throughout the semester and building up to the design of a RISC 32-bit pipelined microprocessor that implements a subset of the MIPS instruction set. Laboratories will also involve the use of computer architecture simulators. The intent of the assignments is to increase the student's experience in creating, implementing, and testing complex designs.

Homework Problems: There will be approximately 4 homework problem assignments consisting of questions from the textbook. These questions are selected to reinforce course material and prepare students for exam questions.

Lab Assignment and Homework Problem Submissions: All assignment reports and homework submissions will be submitted via E-Learning in PDF format and all other files (e.g., code, waveforms, etc.) will be submitted in the appropriate format based on the tools used. *These files may not be submitted as PDF*. This means you will need to either prepare these submissions electronically or scan your handwritten submissions for electronic submission. Physical paper submissions will not be accepted. ***Late assignments will not be accepted!*** Please refer to the class policies document for additional information on academic honesty policies.

Computer usage: You will use Quartus for the laboratories and VHDL designs, and a Web-accessible portal to access computers architecture simulators. Detailed instructions will be given in an assignment.

Exams: There will be two midterm exams: the first one about half way through the semester and the second one on the last day of class.

Grade: The grade will be calculated by the following weights:
Assignments - 55%
Homework – 10%

Midterm 1 – 15%
Midterm 2 – 20%

Final letter grade assignments will be determined based on the standard 90/80/70/60 break down with +/- grades assigned for the upper/lower 2.5%, respectively. Refer to this site for University grading policies: http://www.registrar.ufl.edu/catalog/policies/regulationgrades.html

Approximate Course Outline: Refer to the course calendar for details (subject to change): *Note: since the lab structure of this semester's offering is changing, this schedule is not accurate at the time of posting and will be changed throughout the semester, however, all topics listed will be covered at some point during the semester, only the ordering will change.*

Weeks 0-1:	Introduction. Components of a computer system. Evolution of technology.
Week 2:	Instruction set architecture design and hardware/software interface.
Weeks 3-5:	Organization of single- and multi-cycle RISC microprocessors. Datapath and control logic. Introduction to the design of key datapath components (ALU, registers, shifters, signextenders) using VHDL behavioral and structural descriptions. Micro-programming.
Week 6:	Performance: measurement, metrics, summarization and interpretation.
Week 7:	Number systems: representation and operations; fixed and floating-point implementations.
Weeks 8-9:	Pipelining. Data hazards and forwarding. Superscalar design.
Weeks 10-11:	Memory hierarchies, caches: organization, implementation and performance.
Week 12:	Virtual memory: address translation, placement, look-aside buffers.
Weeks 13-14:	Input/output. Disk technologies, busses and protocols. I/O system design. Redundant arrays of inexpensive disks (RAID).
Week 15:	Advanced topics.
Throughout the semester:	Guest speakers, company representatives, etc.