Course Syllabus

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Schedule:

MWF 7th period 1:55 – 2:45 pm, PSY 0130
LAB TBD

Instructor:

Dr. David Cheney
djcheney@ufl.edu
NPB 2232 x2-7545, NSC(TBD), & NEB229
Office Hours: M8th, WF6th Period in NEB229

TA:

Mason Rawson
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Office hours: TBD

Quincy Flint
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(mailto:qflint@ufl.edu) Office hours: TBD

Text:

"Computer Organization & Design", Patterson & Hennessy, Morgan-Kaufmann,
5th edition, ISBN 0124077269 (The white one with the orange spine)

Topics Covered:

Fundamentals in design and quantitative analysis of modern computer architectures and systems, including instruction set architecture, basic and advanced pipelining, superscalar and parallelism, memory hierarchy, and storage.

Prerequisites:

EEL3701C and EEL 4712: Combinational and sequential logic design principles, advanced modular design logic, finite state machines, and binary logic. Competence in programming with a hardware description language (VHDL or Verilog) is required.

Lab Assignments:

Assignments consisting of questions covering the material discussed in class and design laboratories will be posted on the web and announced in class. There may be as many as six assignments. These laboratories consist of coding a MIPS assembler/disassembler and designs implemented in Verilog, increasing in complexity throughout the semester and building up to the design of a RISC 32-bit pipelined microprocessor that implements a subset of the MIPS instruction set. The intent of the assignments is to increase the student's experience in creating, implementing, and testing complex designs.

Homework Problems:

There will be four homework problem assignments. These questions are selected to reinforce course material and prepare students for exam questions.

Lab Assignment and Homework Problem Submissions:

All assignment reports will be submitted via Canvas in PDF format. This means you will need to either prepare these submissions electronically or scan your handwritten submissions for electronic submission. Physical paper submissions will not be accepted. Please refer to the class policies document for additional information on academic honesty policies.

Computer software:

You will use Quartus for the laboratories and Verilog designs. Detailed instructions will be given in an assignment.

Exams:

There will be three exams: one in mid/late February, the second in early April and the third on the last day of class or during the assigned final exam time slot (TBD).

Grade: The grade will be calculated by the following weights:

Assignments – 55%
Homeworks – 10%
Exam 1 – 10%
Exam 2 – 10%
Final Exam – 15%

A = 92 – 100
A- = 90 – 91.99

B+ = 88 – 89.99
B = 82 – 87.99
B- = 80 – 81.99

C+ = 78 – 79.99
C = 72 – 77.99
C- = 70 – 71.99

D+ = 68 – 69.99
D = 62 – 67.99
D- = 60 – 61.99

Less than 60 will result in an E grade

Course Schedule

This page was last updated on 1/2/2018

This schedule is subject to change throughout the semester.
Please check back frequently for updates.

Week	Content	Readings	Links
Week 1 Jan 8	Introduction	Chapter 1	
Week 2 Jan 15	MLK Jan 15, No Class Instruction Set Architecture (ISA)	Chapter 2 sections: 2.1-2.8, 2.10-2.13, 2.17-2.20	
Week 3 Jan 22	ISA Single Cycle Datapath		
Week 4 Jan 29	Single Cycle Datapath Single Cycle Control	Chapter 4 sections: 4.1-4.4	
Week 5 Feb 5	Single Cycle control Multicycle Processor	Chapter 4 sections: 4.5-4.9	
Week 6	Multicycle Processor		

Feb 12	Pipelining Pipeline Hazards		
Week 7 Feb 19	Pipeline Hazards EXAM 1, Feb 23		
Week 8 Feb 26	Performance Multipliers and Shifters	Chapter 3	
March 5	Spring Break No Classes		
Week 9 Mar 12	Multipliers and Shifters Division and Floating Point	Chapter 5 sections:5.1-5.4,5.8-5.9	
Week 10 Mar 19	Division and Floating PointMemory Hierarchies	Chapter 5 sections:5.6-5.7	
Week 11 Mar 26	Memory Hierarchies	Section 5.4	
Week 12 Apr 2	Memory Hierarchies Exam 2 review EXAM2, April 6		
Week 13 Apr 9	Virtual Memory Parallel Computing		
Week 14 Apr 16	Instruction Level Parallelism Thread Level Parallelism Data Level Parallelism	Section 2.11. 3.6, 4.10, 5.10- 5.11, 6.1-6.3	
Week 15 Apr 23	Dynamic Scheduling Tomasulo's Algorithm GPU's	Section 6.4, 6.6	
Finals Week Apr 30	Final Exam Apr 30 7:30AM-9:30AM		

Course Summary:

Date	Details