Course Syllabus

Course Number & Name: EEE 4329 / 5400 - Future of microelectronics circuits
(Spring 2023    CLASS on EDGE Lectures on E-Learning)

Credits and Contact Hours: 3 crs; 3 classes per week of 50 minutes each
Class period: 7th (1:55 to 2:45pm )

Instructor’s or Course Coordinator’s Name: Dr. Scott E. Thompson
Instructor Prof. Scott Thompson
535 Engineering Bldg
846-0320
Office hours: MWF 8th period
Plus e-learning discussion board (https://lss.at.ufl.edu/)
(Plus welcome additional office hours arranged email thompson@ece.ufl.edu)
(Please stop by to talk about class or career or any topic of interest)

Textbook Title, Author, and Year: Nanoelectronics and Information Technology 2003 or equivalent. Textbook OPTIONAL

1. Supplemental Material: ~35 journal papers and handouts

Specific Course Information

1. Catalog Description: Analysis and design of possible future transistor technology to fabricate microelectronics circuits
2. Prerequisites or Co-requisites: Electronics I, Solid State Devices, Basic knowledge of semiconductor physics and devices. The class will be introductory and targeted towards students with a diverse background from electronics to material science. The class will be designed to introduce CMOS, non classical CMOS, and post CMOS device concepts without a quantum mechanical background.
3. Required, Elective, or Selected Elective (Table 5-1):

Specific Goals for the Course

1. Specific Outcomes of Instruction:

This course focuses on analysis and design transistors for the fabrication of future microelectronic circuits and memory. A very brief introduced and described CMOS digital and memory technology will be introduced along with Moore’s law and scaling
trends. Next class will most of the time on analysis of potential technologies to replace Si CMOS transistors.

1. Explicitly indicate which of the student outcomes listed in Criterion 3 or any other outcomes are addressed by this course:

   EE2, a, c, e, l, k

**Brief List of Topics to Be Covered**

**Week 1 Logic Technology Roadmap**

- Past: BJT, planar NMOS, planar CMOS, FinFET
- Technology nodes 22nm to 1nm
- Overview Planar, FinFET, GAA, CFET
- Overview Standard cells and logic density

**Week 2:** Nanowires, Nanosheets and CFET

**Week 3:** Burried power rails

**Week 4:** Start of the art DRAM

**Week 5:** State of the NAND FLASH

**Week 6a** Introduction to SEMulator3D software

**Week 6b** CMOS Image Sensors and 3D cameras

**Week 7** Carbon nanotube Transistors

**Week 8** Advanced Device Concepts / Nanofabrication limits

- Lithography
  - 193i, EUV
- Devices limits: mobility, velocity saturation, quantum-statistical

**Week 9.** Resistive RAM, PCRAM and Cross point 3D memory

**Week 10:** MRAM and Universal Memory

**Week 12** DRAM and Moore’s Law Revisited

- Post conventional CMOS, DRAM and NAND technologies
- Gate all around CMOS, III-V material, 3D,
- Carbon nanotubes transistors
- Single electron devices for Logic applications
- Other??
Week 14 Next wave of computing (internet of things / wearable electronics)

- Near threshold computing?

Week 15 Single Electron Devices

Week 16: Future Careers / Final Project

- Grading:
  - 100 points Exam 1 Wednesday Feb 10
  - 100 points Exam 2 Friday March 24

100 points Exam 3 Friday April 14

- 30 points homework
- 50 points class project: SEMulator3D software
- 150 points Comprehensive Final 5/04/2023 3:00 - 5:00

- No exam make-up unless valid excuse. All valid excuses must be approved by the Professor.
- Final Grading Scale

- A 100% to 94%, A- < 94% to 90%, B+< 90%to 87%, B< 87% to 84%
- B-< 84% to 80%, C+< 80% to 77%, C< 77% to 74%, C-< 74% to 70%
- D+< 70% to 67%, D< 67% to 64%, D-< 64% to 61%, E< 61% to 0%
- Attendance: Due to quantity and research nature of material, it is important to make every attempt to attend class or watch all class lectures. Class attendance is required on days I announce class discussions.